Product Description

2.1 Introduction

The LeCroy Model 1881 provides 64 channels of analog to digital conversion in the FASTBUS format. It is designed for elementary particle and nuclear physics experiments and was developed to meet the fast converison time needs of modern experiments. Its conversion time is well matched with that of the 1872A, 1876 and 1877 Time to Digital converters for very fast total system throughput. The 1881 is also compatible with the LeCroy 1810 Calibration and Timing (CAT) module to simplify the implementation of multiple module systems. The measurement in the 1881 is performed using the MTD132A and the MQT200S, full custom ASICs developed by LeCroy Corporation.

2.2 Product Description

The 1881 Analog to Digital Converter offers all the flexibility of the 1880 series Analog to Digital converters but with a 15 us conversion time for all 64 channels. It has 100 fC least count with a full 12 bits of dynamic range above pedestal for each channel. Pedestal values range from 15 pC to 75 pC. Permissible gate widths may vary from as little as 50 ns to as much as 500 ns. Each 1881 has 64 channels of front panel input and a single gate input. Events are stored in an on-board sixty four event cyclic buffer memory. A pedestal memory permits the loading of a separate pedestal value for each channel, which is used to suppress unwanted data. Both front panel control inputs are differential ECL (dECL) and are terminated by a balanced 102 ohm impedance matching network. The terminations may be disconnected using jumpers to allow daisy chaining of modules.

Operation of the 1881 can be thought of in four phases: programming, acquisition, conversion and readout. Once the control and status registers have been properly programmed, the module is in acquisition mode and ready to accept a gate pulse. The duration of the gate pulse defines the acquisition phase. The gate may be provided either via a front panel dECL input, via the 1810 CAT module, or a nominal 500 ns pulse triggered by a write to CSR #0 <7>. For the duration of this gate signal, each of the 64 individual inputs integrate the charge applied to them. Immediately following this acquisition phase, the data is converted to a digital representation and then placed in a multi-event buffer to await readout. If sparsification is selected, data is discarded from channels that are below their individual thresholds. The data is thus 'sparsified' (also known as zero suppresion) so that signals on the front end inputs less than the programmed threshold values are not buffered; it is thus not necessary to transmit unwanted data over FASTBUS.

A fast clear may be applied to the module any time from 100ns after the end of the gate until the end of the Fast Clear Window (FCW). If a fast clear is applied during this period the event currently being converted will be discarded. It is important to realize that setting the FCW to longer than 14 us will increase the conversion time of the module to FCW + 1us. If an external FCW is selected from the CAT then an FCW of less than 14 us from the end of the gate will cause an internal FCW of 14 us with a corresponding conversion time of 15 us. There is no restriction within the 1881 of the maximum FCW that may be applied externally.

The data of the 1881 is stored as a 32 bit word. These include data, channel number, the geographic address and a word parity bit. The functionality of the 1881 can be tested using an internal tester in conjunction with a 1810 CAT module. The module does not provide any trigger outputs

2.3 Specifications

Please refer to the model 1881 technical data sheet for a complete summary of all relevant specifications.

2.4 Front Panel

The LeCroy Module 1881 ADC front panel provides the user with connectors for easy system integration and LEDs to indicate status. Cables necessary for proper installation can be purchased from LeCroy. See Section 3.2 for more information regarding cabling.

2.4.1 Displays

Two colored LEDs exist on the front panel of the 1881 to indicate the status of operations. The LED outputs are pulse stretched for visibility.

- **Slave Addressed LED:** As per the FASTBUS specification, this yellow LED is lit whenever the ADC module is address locked. It should be noted in some early boards this LED will not light when the module is addressed using a FASTBUS Broadcast.

- **GATE LED:** This green LED is illuminated whenever the ADC registers a gate. The gate may come via the front panel input marked **Gate**, it may come from the 1810 CAT module, or it may come from a write to CSR #0 <7>. It should be noted in some early boards this LED is only edge triggered, if the GATE is locked on the light will pulse and then extinguish.

2.4.2 Inputs

All analog inputs are received via four 34 pin connectors. A 3M connector type 3414-6034 or a LeCroy connector part number 403 220 034 with pull tab part number 403 910 034 will mate with the ADC header and provide strain relief. The bottom two pins of each of the four headers are connected to the clean analog ground within the module. The analog inputs are numbered from top to bottom in ascending order.

- **IN:** 64 inputs used to receive individual channel signals. It is recommended the source's output DC impedance exceed 1 Kohm for each of these signals to avoid excessive pedestal spread and degraded temperature performance. The inputs may be configured in several different modes. These include 50 ohm single ended, 100 ohm differential and 100 ohm pseudo-differential. It is important to verify the jumper links (see Section 3.4) are correctly configured.

All front-panel control inputs to the 1881 are differential ECL compatible with the ECLine standard. All control inputs are differentially received. Each pair of differential inputs is terminated with an effective 102 ohms. Two control inputs are differentially received via an 6 pin header located at the bottom of the front panel.

The control signals can be connected by single pair headers AMP part number 5-87456-2. A brief description of each input follows below:

- **CLR:** A dECL input used to issue fast clears to the module. A clear pulse can be issued at any time during the FCW provided it is at least 100 ns wide. When a clear is issued, the data of the current event is cleared and the module returns to acquisition mode 1 us after the trailing edge of the pulse. The control and status registers are not affected by a clear. This signal may also be applied by writing CSR #0<31> or from the 1810 CAT via TR7. Note all the clear sources are simply OR'd.

- **GATE:** A front panel dECL input which receives the gate input pulse. This signal defines the time during which charge will be integrated on each of the 64 **IN** inputs. The gate pulse may also be applied from the 1810 CAT module via TR6 on FASTBUS. The source is selected using CSR #1 <1>. The test gate generated by a write to CSR #0 <7>it is ORed with the selected source. It should be noted that if the selected gate source is high this will cause internal gates not to function.

2.4.3 Outputs

The front panel CIP (Conversion in Progress) output from the 1881 is differential ECL compatible with the ECLine standard. Each of differential outputs is pulled down with 300 ohms to -5.2 V. If the CIP signal is used, it should be terminated at the receiving end in 100 ohms. The best method of doing this is to connect two 51 ohm resistors in series across the signal at the receiver and connect the center tap via a 0.1uF capacitor to ground. If LeCroy ECL line products are used to receive the signal the termination is already included internally. Differential ECL cannot be Wire Or'd.

- **CIP:** Conversion in Progress (CIP) is a single dECL signal provided to aid in the gating logic. While CIP is true, the unit is not capable of accepting a new gate, and the data from the previous event is not guaranteed to be ready for readout via FASTBUS. It should be noted that if an extended FCW is used this will delay the end of CIP. It is the users responsibility to

ensure that GATEs are NOT issued during CIP.

2.5 Control and Status Registers

Seventy control and status registers (CSR) are implemented in the 1881: CSR #0, CSR #1, CSR #3,CSR #5, CSR #7, CSR #16, and CSR $C0000000_h$ - $C000003F_h$.

2.5.1 Control and Status Register 0

Functions necessary even for the simplest of operations are contained in CSR #0. In order to implement these functions most economically, the definition of the bits for CSR #0 are not the same for Read and Write operations. Some bits are inherently meaningful only for write operations, because their status can only be altered by writing to another bit in the register. Other bits, such as the module identification bits, are only meaningful for read operations. When read, the 1881 presents $104B_h$ on the Address/Data bus lines 16–31 as its manufacturer's identification. CSR #0 is the default register when a primary address to control space is issued. See section 2.6 for more information regarding addressing. See Figures 2–1 and 2–2 for individual bit definitions.

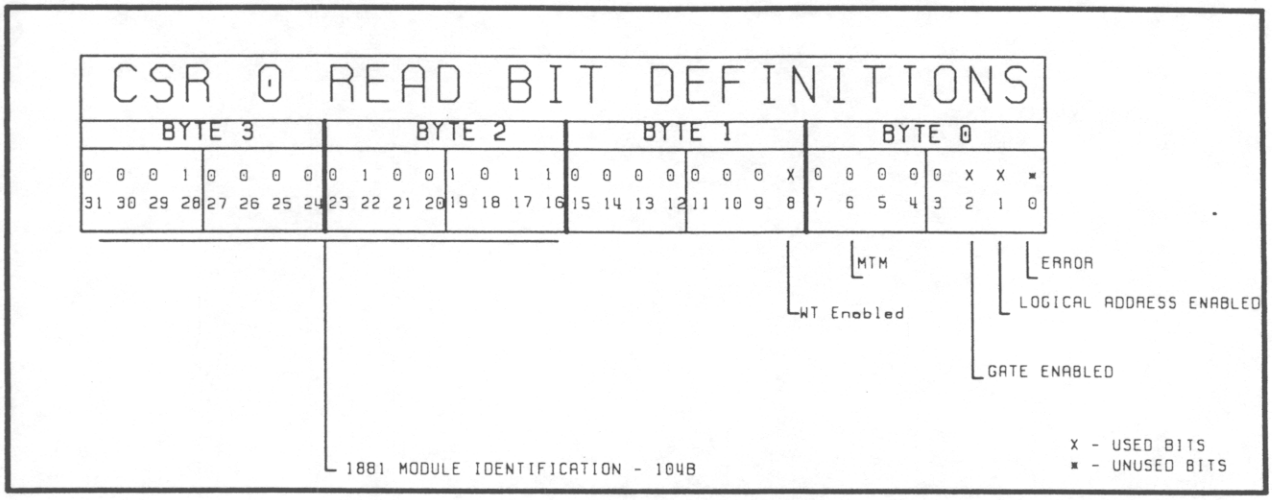

Figure 2–1 CSR #0 Read Bit Definitions

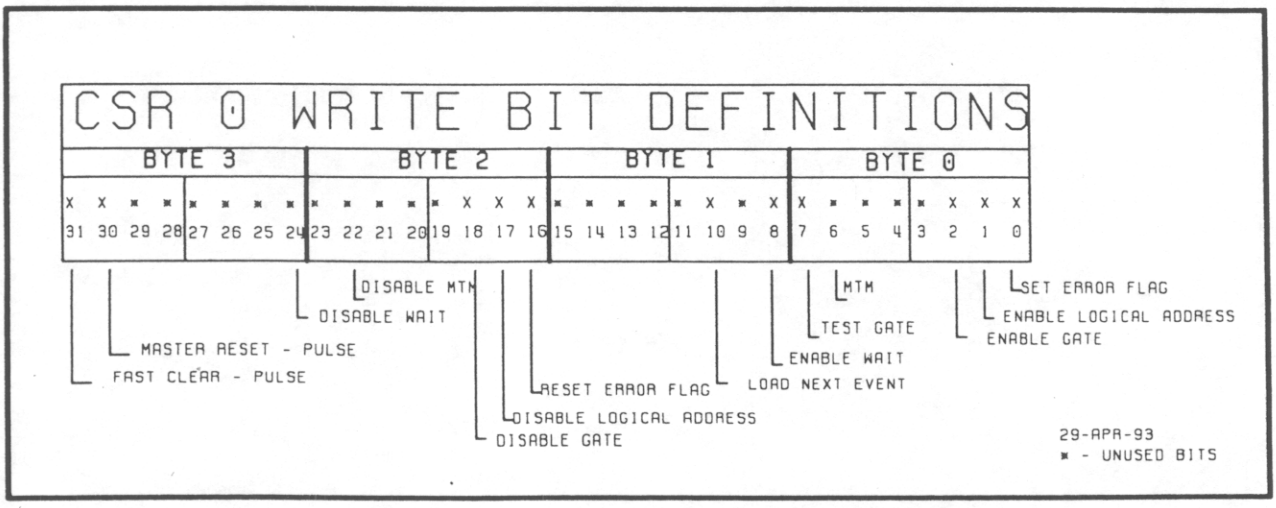

Figure 2–2 CSR #0 Write Bit Definitions

CSR #0 After Master Reset or Power–up - $104B\ 0000_h$

- **FAST CLEAR:** abort conversion and buffering of the last event. The prefered method of clearing the unit is via a CAT or front panel input as the FAST CLEAR must occur during the FCW which is difficult to guarantee if carried out over FASTBUS.
- **MASTER RESET:** Returns the module to its power-up configuration. All CSRs are returned to their power-up states. This is the easiest method of resetting all the output buffers in a crate if the system goes out of step.
- **LOAD NEXT EVENT:** Advances Read pointer (this is the data space NTA when MTM is set) to first location of next event, then copies word count from header word of that event to CSR #5. This makes the 1881 ready for a block transfer to readout one entire event.
- **ENABLE WAIT:** If this bit is set then readout during conversion is disabled. If a FASTBUS cycle to the buffer memory occurs during conversion then the FASTBUS WT line will be asserted until the end of conversion. In most cases this option should be used.
- **TEST GATE:** A write to this bit is intended only for confidence testing and will generate a nominally 500 ns gate pulse. The enable test pulse bit CSR #1 <29> must be set if a programmable amplitude test pulse is desired.
- **MTM**: Memory test mode allows the direct addressing of the buffer memory using the data space NTA (normally writes to data space NTA are ignored.). When this bit is clear the 1881 acts as a FIFO (First In First Out) from DSR #0.
- **GATE ENABLE:** This bit must be set to enable the module for data acquisition.
- **ENABLE LOGICAL ADDRESS:** This bit must be set for the module to respond to the logical address as stored in CSR #3. This bit also selects which address is included in the data header word.
- **SET ERROR FLAG:** Sets the error flag

2.5.2 Control and Status Register 1 – Configuration

The acquisition configuration of the module is primarily defined in CSR #1.

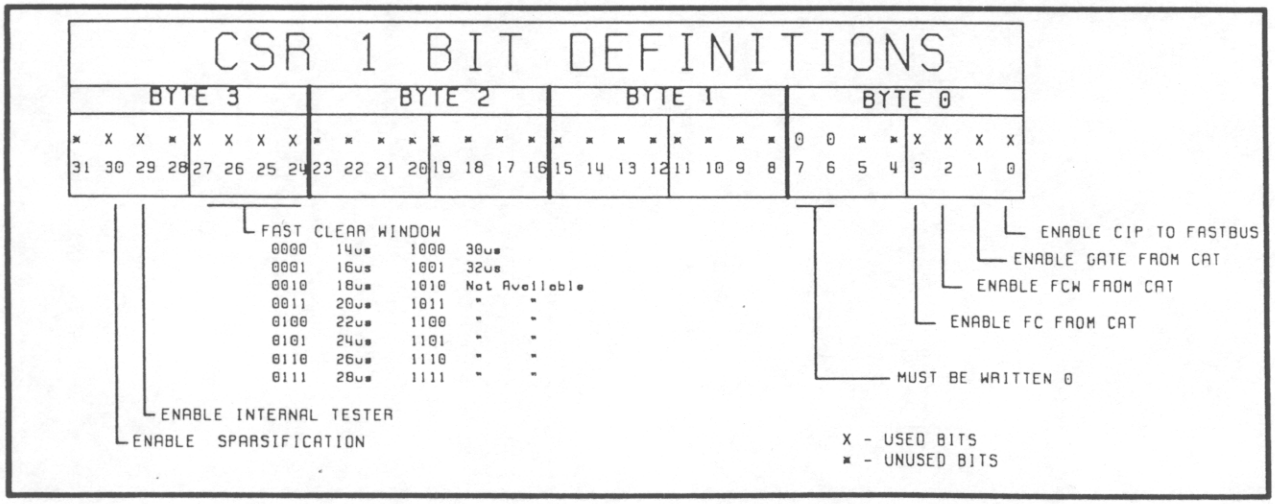

Figure 2–3 CSR1 Bit Definitions

- **ENABLE SPARSIFICATION**: Setting this bit causes data values which are less than the threshold for the corresponding channels to be discarded during conversion. Only those data values which exceed their respective thresholds are written to the buffer. CSR #C0000000$_h$ – CSR #C0000003F$_h$ contain the thresholds for channels 0 – 63 respectively. If this bit is reset (the

power up state) the unit will always readout 64 events.

- **ENABLE INTERNAL TESTER**: This bit must be set for the internal tester to be operative. If set a level on UR0,UR1 provided normally by the 1810 CAT will determine the amplitude of a test pulse applied to all channels.

- **FAST CLEAR WINDOW:** Bits <27:24> determine the length of time the on-board timer permits the user to issue a fast clear to the module after the end of acquisition. The fast clear window begins immediately following the end of the gate. For the on-board FCW to be used the 1810 CAT FCW must be disabled (CSR #1 <2> = 0). Once the fast clear window has ended, the current event is placed in the multiple event buffer and must either be read out or skipped. When read, the status of the bits is presented.

CSR #1 After Master Reset or Power-up - 0000 0000_h

2.5.3 Control and Status Register 3 - Logical Address

CSR #3 is used to designate the logical address to which the module will respond. <31:16> are available to write the logical address. <15:0> will not write and will always read as 0. CSR #3 is cleared after power up but is not reset by Master Reset.

2.5.4 Control and Status Register 5 - Word Count

CSR #5 is implemented as a 7 bit read/write register. It selects the number of words that will be transferred on a subsequent block transfer. After the block transfer it will be reset to zero. Load next event (LNE) will automatically load register 5 with the number of words in the next event. Bits <31:16> are not defined for read. CSR #5 is neither used nor modified with FASTBUS random reads to data space.

2.5.5 Control and Status Register 7 - Broadcast Classes

This register, CSR #7, is used to specify the broadcast classes to which an 1881 will respond. It is implemented as an 4 bit read/write register. Bits 3 through 0 correspond to broadcast classes 3 through 0 respectively. If bit N is set the 1881 will be selected by a broadcast to class N devices.

2.5.6 Control and Status Register 16 - Buffer Status

CSR #16 is implemented as a 16 bit read-only register used to indicate the location of the read and the write buffer addresses. CSR #16 <13:8> indicate the next buffer to be readout, and CSR #16 <5:0> indicate the next buffer address to be filled. CSR #16 is set to $3F00_h$ on power up and after master reset.

2.5.7 Control and Status Registers C0000000h - C000003Fh

These 64 read/write registers are used to program the threshhold settings for each of the input channels. If during buffering a given channel's data value is less than its threshold setting, that data will not be buffered. The threshold is NOT subtracted from the data written into the buffer. The threshold value RAM is 16 bits wide and is accessed via the low 16 bits of CSR $C0000000_h$ - $C000003F_h$. The upper 16 bits will be ignored on write and always readback as zero. These CSR's are NOT cleared by powerup or Master Reset.

2.6 FASTBUS Operations

2.6.1 FASTBUS Address Cycles

The 1881 ADC responds to all three primary addressing schemes - geographical, logical and broadcast.

2.6.1.1 Logical Addressing

The 1881 will respond to logical addresses in both CSR and DSR space. The logical addresses to which it will respond are programmed in CSR #3.

2.6.1.2 Geographical Addressing

On each segment the first 32 logical addresses are reserved for positional addressing of devices. The next 192 logical addresses are reserved.

2.6.1.3 Broadcast Addressing

- **1_h :** General Broadcast. All devices respond to subsequent data cycles.
- **5_h :** Only devices of class N respond to subsequent data cycles.
- **9_h ,BD_h :** Sparse Data Scan: Devices respond by asserting TPin during following read cycle if at least one event is in the buffer. 0xBD is specific to LeCroy modules. This is determined by comparing the read and write pointer (write == read + 1 indicates empty). It should be noted that after an LNE this broadcast will return false if the next event was the only one.
- **19_h :** Sparse Data Scan: Devices respond by asserting TPin if they have an empty set of buffers. (inverse of 9_h ,BD_h).
- **D_h :** Devices respond by asserting TPin during following read cycle.
- **CD_h :** Only boards with CSR5 not equal to 1 assert TPin during following read cycle. This broadcast can be used IMMEDIATELY after a LOAD NEXT EVENT to determine whether the current event has more than just the header word in it. That is, at least some data was greater than its sparsification threshold

2.7 Data Space

In normal operation a data space NTA is not implemented. All data is accessed by FASTBUS BLOCK reads from data space (NTA is ignored though as per FASTBUS specification reads and writes to it are acknowledged normally.) The buffer appears to the user as a FIFO. The FIFO only advances to the next word within an event after each cycle of a FASTBUS BLOCK read. It should be realized that the FIFO readout is limited to ONE event. In order to advance to the next buffer a Load Next Event (LNE) is required.

Data resulting from an event is stored in sixty four 128 word buffers. Each of these event buffers is a RAM, thus in Memory Test Mode (MTM) any address may be randomly read or written via standard FASTBUS data cycles. Each event buffer contains enough words to hold the maximum data resulting from a single event (65 words). An event is defined as the occurance of one gate.

The data storage area acts as a circular buffer. CSR #16 specifies both the next event buffer to be filled and the next event buffer to be read. The next event buffer to be read can be modified by issuring a LNE or in MTM via the Next Transfer Address (NTA). When a master reset is issued, or at power-up, the next event buffer to be read will be 63, and the next event buffer to be filled will be 0. Before readout of the first event can occur, a LNE command must be issued.

Address 0 of each page contains the word count for that event. It is automatically loaded into CSR #5 when a load next event command is issued. After each FASTBUS block transfer data cycle, the word count register is decremented.

2.7.1 Data Word Format

The 1881 data is read out as a 32 bit data word.

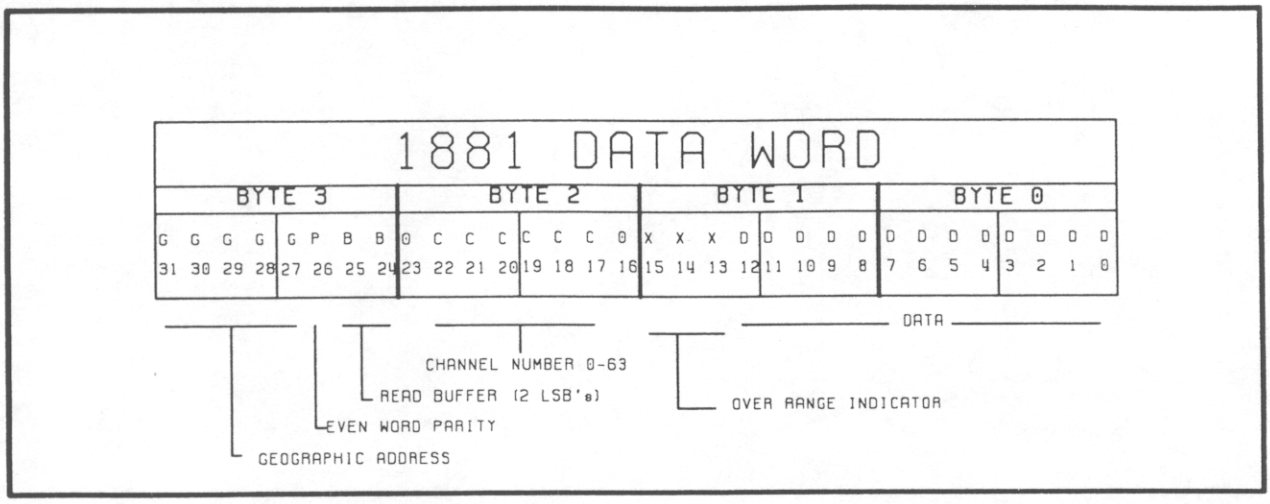

Figure 2–4 1881 Data Word Format

- EVEN WORD PARITY: The total number of 1's within each 32 bit data word (including the EVEN WORD PARITY bit) will always be even.
- GEOGRAPHIC ADDRESS: Identifies board's physical location within the FASTBUS crate.
- READ BUFFER: This two bit field shows the 2 lsb's of the buffer being read out. The intention of theses bits is to check synchronization between boards on readout.
- CHANNEL NUMBER: Identifies the channel number being read out.
- OVER RANGE INDICATOR: These bits will normally be zero. If a substantially overange input is converted they will all read as 1. It should be noted that these bits being zero is not a sufficient indication that a valid level input has been converted. If they are zero then only signals up to 4096 + intrinsic pedestal will be measured to within the specified limits.
- DATA: These bits indicate the converted input value. If the OVER RANGE INDICATOR bits are high then the data bits will also be high. The data is NOT pedestal subtracted.

2.7.2 Header Word Format

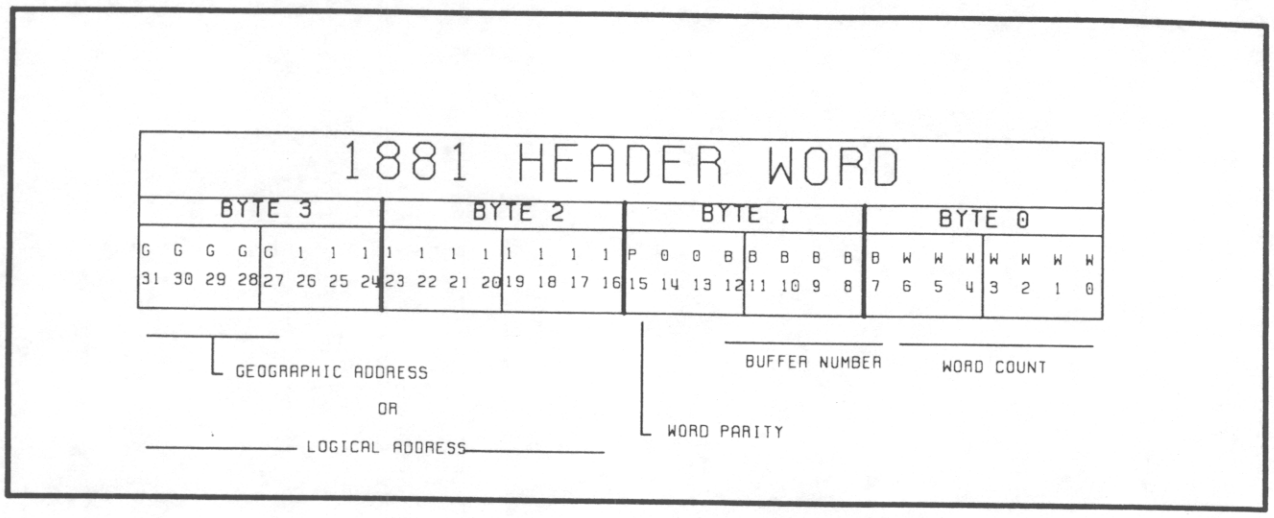

Figure 2-5 1881 Header Word Format

- GEOGRAPHIC ADDRESS: Identifies board's physical location within the FASTBUS crate. The geographic information ONLY will normally be provided. If logical addressing is selected CSR #0 <1> then the geographic information will not be provided.
- LOGICAL ADDRESS: CSR #3 <31:16>. These bits can be used to identify the specific module's data. This information is only provided when the module is in enabled for logical addressing.
- WORD PARITY: The total number of 1's within the header word (including the WORD PARITY bit) will always be even.
- BUFFER NUMBER: Can range from 0 to 63 and indicates position of the buffer containing the header word.
- WORD COUNT: Indicates the number of data words (including the header) contained within thia header word's buffer. It may contain between 1 (all data words below their respective sparsification threshold) and 65 (all data words above their respective thresholds)

2.8 Allocation of the Restricted Use Lines

- TR0: Fast clear input, typically from 1810 CAT
- TR1, TR2: Gate input form FASTBUS (TR1 +, TR2 -) typically from 1810 CAT
- TR5: FCW input from 1810 CAT. Note this may also be referred to as the measurement pause interval (MPI).
- TR7: CIP output to FASTBUS. Note this usage of TR7 is incompatible with 1810 CAT so if a CAT is to be used this output MUST be disabled by CSR #1 <0>=0.
- UR0: clean ground from 1810 CAT. Used as relative ground for UR1.
- UR1: DC reference level used by internal tester to set amplitude of test pulses. This is typically generated by the 1810 CAT. The full scale is +10V.